A 26dB Gain, 100GHz Si/SiGe Cascaded Constructive Wave Amplifier

James F. Buckwalter and Joohwa Kim
University of California, San Diego

The availability of W-band (75-111GHz) silicon integrated circuits will potentially revolutionize medical and security imaging, as well as high capacity wireless communications. Traditional W-band circuits rely on GaAs or InP devices, but recent work demonstrates silicon front-ends for W-band imaging and communications [1][2] although low intrinsic bandwidth of silicon devices presents performance limits compared to III-V processes. At millimeter-wave frequencies, new challenges exist for silicon wideband circuits [3][4][5]. In this work, we present an amplifier topology - the Cascaded Constructive Wave Amplifier (CCWA) - that combines features of traveling wave and cascaded amplifiers for millimeter-wave applications.

The CCWA topology is shown in Figure 1, and is based on the cascade of identical traveling wave stages. These stages support forward and backward traveling waves since the input and output are electrically connected through a transmission line. Each stage employs shunt-shunt active feedback to tap the output and circulate it back to the input of the stage. In contrast to distributed amplifiers, the gain of this amplifier is cascaded rather than distributed, i.e. $G \propto N$ rather than $\log N$, and therefore achieves higher gain than distributed amplifiers. Additionally, the bandwidth is large because of the broadband matching of the stage and has similar benefits to those of distributed circuits.

Confidential: Accepted to ISSCC 2009.
An important feature of the CCWA topology is amplification of the forward traveling wave and isolation of the backward traveling wave. The mechanism that provides constructive interference of the forward wave and destructive interference of the backward wave is the shunt-shunt active feedback illustrated in Figure 2. The active feedback cascades the emitter follower devices, Q2 and Q3, and common emitter device, Q1. The emitter follower increases the collector-emitter voltage of Q1 and increases the input impedance to minimize the loading of the base-emitter capacitance of Q2. Additionally, the base-collector capacitance of Q1 terminates into the high-impedance node between the emitter follower and common emitter amplifier. Q1 is degenerated to decrease the shunt conductance on the input, thereby minimizing loading on the transmission line.

To analyze the stage, the feedback is modeled as a transconductance, $g_m$, modulated by the output voltage and delayed by $T_d$ through the feedback. Studying the incident waves from port 1 and port 2 of the stage under these conditions, transmission parameters, $S_{21}$ and $S_{12}$, are derived in Figure 2. The feedback voltage gain, $A_v$, is the product of the $g_m$ and the parallel line impedance, $Z_0/2$. Most importantly, $S_{21}$ and $S_{12}$ depend on the signal phase through the transmission line, $\theta$, and $T_d$. Constructive interference of the forward traveling wave and destructive interference of the backward traveling wave occur when

$$\theta + \omega T_d = \pi \quad \text{and} \quad \theta - \omega T_d = 0. \quad (1)$$

Therefore, the transmission line and feedback delay should be a quarter wavelength at the amplifier center frequency. Under these conditions, amplification of the forward traveling wave and isolation of the reverse traveling wave is possible with $A_v$ per stage less than unity. With the feedback gain less than one, the stability of the stage can be guaranteed. The feedback gain is confidential: Accepted to ISSCC 2009.
chosen by degeneration through $R_E$. In this design, $Q_1$ is biased for $g_m$ of 60mS while $R_E$ is 70Ω. Therefore, the feedback gain is ideally $A_v = 0.27$. In Figure 3, the S-parameters for a single stage are plotted for $A_v = 0.25$. $S_{21}$ reaches a gain of 2.3dB while $S_{12}$ is -3dB. Additionally, the predicted input and output return loss are identical and less than -9.8dB. The analysis is extended to the cascade of stages using $ABCD$ matrix techniques. In Figure 3, the S-parameters for $N = 2$ demonstrate the proportional increase in gain and isolation without sacrificing the return loss. In fact, cascading stages improves the stability. In this work, twelve cascaded stages are implemented for a predicted gain of 27dB.

The measurements are performed using Cascade ACP110-LW GSG probes and the Agilent E8361A two-port network analyzer with N5260A mmWave controller. Measured S-parameters are shown in Figure 4. The forward and backward transmission illustrates amplification of the forward wave and isolation of the backward wave. $S_{21}$ reaches a gain of 26dB at 99GHz and has a 3dB bandwidth of 14GHz between 93 and 107GHz. Since the traveling wave is amplified through twelve cascading stages, the average gain of each stage is 2.2dB, agreeing closely with the analysis and simulations. Alternately, $S_{12}$ is -24dB at 99GHz and remains relatively constant across the entire frequency range. The input return loss across the 3dB bandwidth is less than -15dB while the output return loss is -12dB. The output-referred 1dB compression point for the amplifier was -0.1dBm. Simulations indicate that the noise figure of the amplifier is under 13dB at 99GHz.

The nominal gain is measured with a current consumption of 19.2mA from a 2V supply for the emitter follower. The emitter follower current is set by providing $I_{bias} = 2mA$. The common
emitter devices consume a total current of 19.9mA from 2V supply. The overall power consumption of the amplifier is 78mW with an additional 4mW for on-chip bias generation.

The current bias of the emitter follower provides a convenient method to adjust the feedback gain. Reducing the $I_{bias}$ reduces the emitter follower gain and, hence, $A_v$. The gain and bandwidth of the CCWA is shown in Figure 5 as a function of $I_{bias}$ and, consequently, power consumption. The overall gain-bandwidth of the amplifier increases linearly to 290GHz. Additionally, the bandwidth does not change dramatically for bias currents above $I_{bias}$ of 1.8mA.

Finally, the stability of the suggested cascaded traveling wave amplifier is calculated from the S-parameters in Figure 6 and compared with simulation results. Notably, the twelve stage circuit is unconditional stable for forward gain of 26dB. This agrees with the predicted stability at the same gain. Higher gain (~30dB) is measured at the expense of conditional stability.

The circuit is implemented in 0.12μm SiGe BiCMOS. The HBT devices have $f_T$ of 200GHz. The chip microphotograph is shown in Figure 7 and measures 330μm by 1000μm including the pads. The area of a single stage measures 160μm by 60μm. Within a single stage, the shielded coplanar transmission line meanders through a length of 220μm. This structure is area efficient and minimizes the distance between the input and output of the stage. In conclusion, the CCWA topology is based on cascaded traveling wave stages that offer wideband gain previously unachievable in silicon technologies. The 26dB amplifier provides 7dB more gain than recent W-band work in 0.12μm SiGe [3].

Confidential: Accepted to ISSCC 2009.
Acknowledgments

This work was supported through a DARPA Young Faculty Award under the management of Dr. Michael Fritze. The comments of Professor Larry Larson have been greatly appreciated.

References


Captions

Figure 1. The cascaded constructive wave amplifier schematic.

Figure 2. A single stage of traveling wave amplifier and equivalent circuit.

Figure 3. Simulated S-parameters for a single traveling wave stage and cascade of two stages.

Figure 4. Measured S-parameters for a twelve stage CCWA and simulated S21.

Figure 5. Measured gain and bandwidth as a function of emitter follower bias.

Figure 6. Rollett stability of measured and simulated twelve stage amplifier.

Figure 7. Chip microphotograph of twelve stage cascaded traveling wave amplifier in 0.12μm SiGe BiCMOS.
Figure 1. The cascaded constructive wave amplifier schematic.

Figure 2. A single stage of traveling wave amplifier and equivalent circuit.
Figure 3. Simulated S-parameters for a single traveling wave stage and cascade of two stages.

Figure 4. Measured S-parameters for a twelve stage CCWA and simulated S21.
Figure 5. Measured gain and bandwidth as a function of emitter follower bias.

Confidential: Accepted to ISSCC 2009.

Figure 6. Rollett stability of measured and simulated twelve stage amplifier.
Figure 7. Chip microphotograph of twelve stage cascaded traveling wave amplifier in 0.12μm SiGe BiCMOS.